according to Cutts. There is no teaching or suggestion or even general knowledge in the art that the benefits of a private write memory arrangement in a fault-tolerant redundant configuration are transferable to a system with two independently operating CPUs.

For example, in Nagai, RAM 203 and ROM 204 are dedicated to a tape CPU 201 and RAM 303 and ROM 304 are dedicated to a DRUM CPU 301. These memories are local to, and accessible only by, the CPU they are serving. IF RAM 305, on the other hand, appear to be accessible for both read and writes by the CPU 201, 301. The cited references fail to teach or suggest a modification of the memories 203, 204, 303, 204 to be write-accessible only locally but read-accessible globally.

In view of the above, this application is now in condition for allowance, and an early notice to that effect is earnestly solicited. If the Examiner has any questions or comments, the Examiner is invited to contact the undersigned at the telephone number below.

Respectfully submitted,

Aug. 27, 1996
Date

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